In the Claims:

Please amend claims 1, 6, and 13. The claims are as follows:

1. (Currently amended) A method of forming a semiconductor structure, comprising the steps of:

providing a semiconductor region;

forming a gate stack on top of the semiconductor region, the gate stack including

(i) a gate dielectric region on top of the semiconductor region,

(ii) a first gate polysilicon region on top of the gate dielectric region, and

(iii) a second gate polysilicon region on top of the first gate polysilicon region, the second gate polysilicon region being doped with a type of dopants; and

forming on a side wall of the gate stack a diffusion barrier region and a spacer oxide region,

wherein the diffusion barrier region is sandwiched between the gate stack and the spacer oxide region, and

wherein the diffusion barrier region is in direct physical contact with both the first and second gate polysilicon regions, and

wherein the diffusion barrier region comprises a material having a property of preventing a diffusion of oxigen-containing materials through the diffusion barrier region.

2. (Original) The method of claim 1, wherein the second gate polysilicon region is doped with n-type dopants

3. (Original) The method of claim 1, wherein the step of forming the gate stack comprises the

steps of:

forming a gate dielectric layer on top of the semiconductor region;

forming a gate polysilicon layer on top of the gate dielectric layer;

implanting the type of dopants into a top layer of the gate polysilicon layer; and

etching away portions of the gate polysilicon layer and the gate dielectric layer such that what remains of the gate polysilicon layer after the step of etching comprises the first and second gate polysilicon regions, and what remains of the gate dielectric layer after the step of etching comprises the gate dielectric region.

4. (Original) The method of claim 1, wherein the diffusion barrier region comprises oxynitride silicon.

5. (Original) The method of claim 1, wherein the step of forming the diffusion barrier region and the spacer oxide region comprises the steps of:

forming the diffusion barrier region at a top surface of the side wall of the gate stack; and

forming the spacer oxide region on top of the diffusion barrier region after the step of forming the diffusion barrier region.

6. (Currently amended) ~~The method of claim 1,~~ A method of forming a semiconductor structure, comprising the steps of:

providing a semiconductor region;

forming a gate stack on top of the semiconductor region, the gate stack including

(i) a gate dielectric region on top of the semiconductor region,

(ii) a first gate polysilicon region on top of the gate dielectric region, and

(iii) a second gate polysilicon region on top of the first gate polysilicon region, the second gate polysilicon region being doped with a type of dopants; and

forming on a side wall of the gate stack a diffusion barrier region and a spacer oxide region,

wherein the diffusion barrier region is sandwiched between the gate stack and the spacer oxide region,

wherein the diffusion barrier region is in direct physical contact with both the first and second gate polysilicon regions, and

wherein the step of forming the diffusion barrier region and the spacer oxide region comprises the step of thermally oxidizing the side wall of the gate stack with the presence of a nitrogen-carrying gas.

7. (Original) The method of claim 6, wherein the step of thermally oxidizing the side wall of the gate stack with the presence of the nitrogen-carrying gas comprises the steps of:

pre-heating the nitrogen-carrying gas; and

thermally oxidizing the side wall of the gate stack with the presence of the pre-heated nitrogen-carrying gas.

8. (Original) The method of claim 6, wherein the step of thermally oxidizing the side wall of the gate stack comprises the steps of:

thermally oxidizing a top surface and the side wall of the gate stack with the presence of the nitrogen-carrying gas so as to form a diffusion barrier layer and a spacer oxide layer on the top surface and the side wall of the gate stack; and

removing a portion of the diffusion barrier layer and the spacer oxide layer at a top surface of the gate stack such that polysilicon material of the second gate polysilicon region is exposed to the atmosphere, and such that what remains of the diffusion barrier layer after the step of removing comprises the diffusion barrier region, and what remains of the spacer oxide layer after the step of removing comprises the spacer oxide region.

9. (Withdrawn) A semiconductor structure, comprising:

a semiconductor region;

a gate stack on top of the semiconductor region, the gate stack including

(i) a gate dielectric region on top of the semiconductor region,

(ii) a first gate polysilicon region on top of the gate dielectric region, and

(iii) a second gate polysilicon region on top of the first gate polysilicon region, the second gate polysilicon region being doped with a type of dopants; and

a diffusion barrier region and a spacer oxide region on a side wall of the gate stack,

wherein the diffusion barrier region is sandwiched between the gate stack and the spacer oxide region, and

wherein the diffusion barrier region is in direct physical contact with both the first and

second gate polysilicon regions.

10. (Withdrawn) The semiconductor structure of claim 9, wherein the second gate polysilicon region is doped with n-type dopants.

11. (Withdrawn) The semiconductor structure of claim 9, wherein the diffusion barrier region comprises oxynitride silicon.

12. (Withdrawn) The semiconductor structure of claim 9, wherein a first thickness of a first region of the spacer oxide region corresponding to the first gate polysilicon region and a second thickness of a second region of the spacer oxide region corresponding to the second gate polysilicon region are substantially identical.

13. (Currently amended) A method of forming a semiconductor structure, comprising the steps of:

providing a semiconductor substrate;

forming a gate stack on top of the semiconductor substrate, the gate stack including

(i) a gate dielectric region on top of the semiconductor substrate,

(ii) a first gate polysilicon region on top of the gate dielectric region, and

(iii) a second gate polysilicon region on top of the first gate polysilicon region, the second gate polysilicon region being heavily doped with a type of dopants; and

forming on first and second side walls of the gate stack first and second diffusion barrier regions and first and second spacer oxide regions, respectively,

wherein the first diffusion barrier region is sandwiched between the gate stack and the first spacer oxide region,

wherein the first diffusion barrier region is in direct physical contact with both the first and second gate polysilicon regions,

wherein the second diffusion barrier region is sandwiched between the gate stack and the second spacer oxide region, ~~and~~

wherein the second diffusion barrier region is in direct physical contact with both the first and second gate polysilicon regions, and

wherein the first and second diffusion barrier regions comprise a material having a property of preventing a diffusion of oxigen-containing materials through the first and second diffusion barrier regions.

14. (Original) The method of claim 13, wherein the second gate polysilicon region is doped with n-type dopants.

15. (Original) The method of claim 13, wherein the step of forming the gate stack comprises the steps of:

forming a gate dielectric layer on top of the semiconductor substrate;

forming a gate polysilicon layer on top of the gate dielectric layer;

implanting dopants into a top layer of the gate polysilicon layer; and

etching away portions of the gate polysilicon layer and the gate dielectric layer such that what remains of the gate polysilicon layer after the step of etching comprises the first and second gate polysilicon regions, and what remains of the gate dielectric layer after the step of etching comprises the gate dielectric region.

16. (Original) The method of claim 13, wherein the first and second diffusion barrier regions comprise oxynitride silicon.

17. (Original) The method of claim 13, wherein the step of forming the first and second diffusion barrier regions and the first and second spacer oxide regions comprises the steps of:

forming the first and second diffusion barrier regions at top surfaces of the first and second side walls of the gate stack, respectively; and

forming the first and second spacer oxide regions on top of the first and second diffusion barrier regions, respectively, after the step of forming the first and second diffusion barrier regions.

18. (Original) The method of claim 13, wherein the step of forming the first and second diffusion barrier regions and the first and second spacer oxide regions comprises the step of thermally oxidizing the first and second side walls of the gate stack with the presence of a nitrogen-carrying gas.

19. (Original) The method of claim 18, wherein the step of thermally oxidizing the first and second side walls of the gate stack with the presence of the nitrogen-carrying gas comprises the steps of:

pre-heating the nitrogen-carrying gas; and

thermally oxidizing the first and second side walls of the gate stack with the presence of the pre-heated nitrogen-carrying gas.

20. (Original) The method of claim 18, the step of thermally oxidizing the first and second side walls of the gate stack comprises the steps of:

thermally oxidizing top surfaces and the first and second side walls of the gate stack with the presence of the nitrogen-carrying gas so as to form a diffusion barrier layer and a spacer oxide layer on the top surfaces and the first and second side walls of the gate stack; and

removing portions of the diffusion barrier layer and the spacer oxide layer at a top surface of the gate stack such that polysilicon material of the second gate polysilicon region is exposed to the atmosphere, and such that what remains of the diffusion barrier layer after the step of removing comprises the first and second diffusion barrier regions, and what remains of the spacer oxide layer after the step of removing comprises the first and second spacer oxide regions.